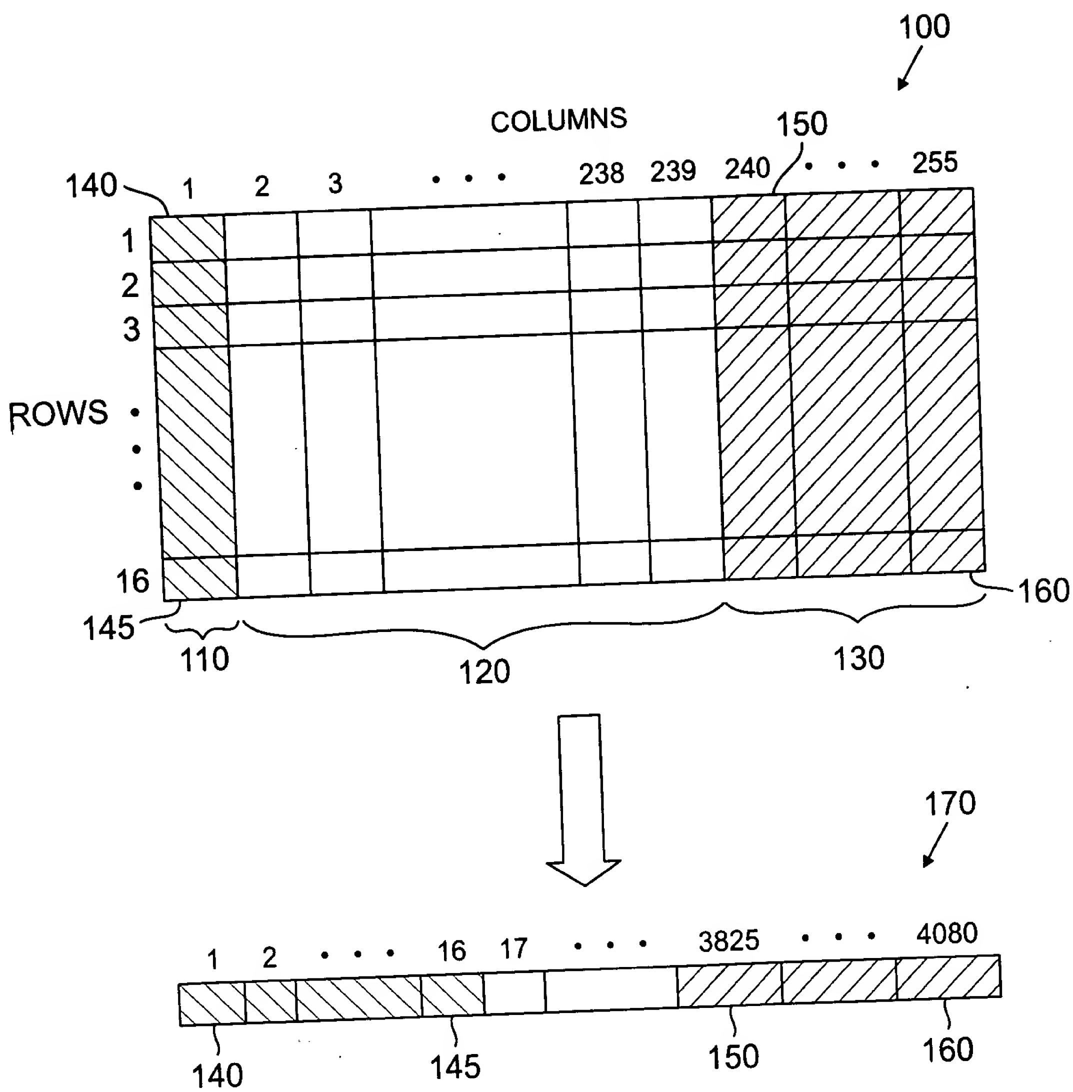


FIG. 1
(PRIOR ART)

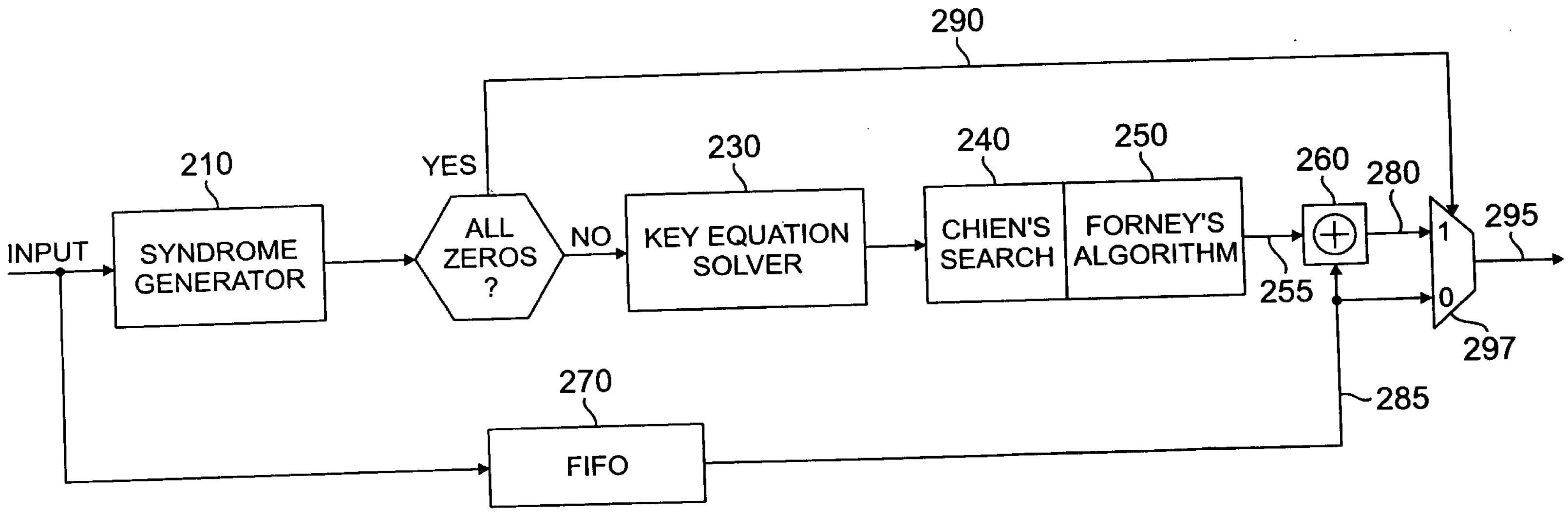


FIG. 2
(PRIOR ART)

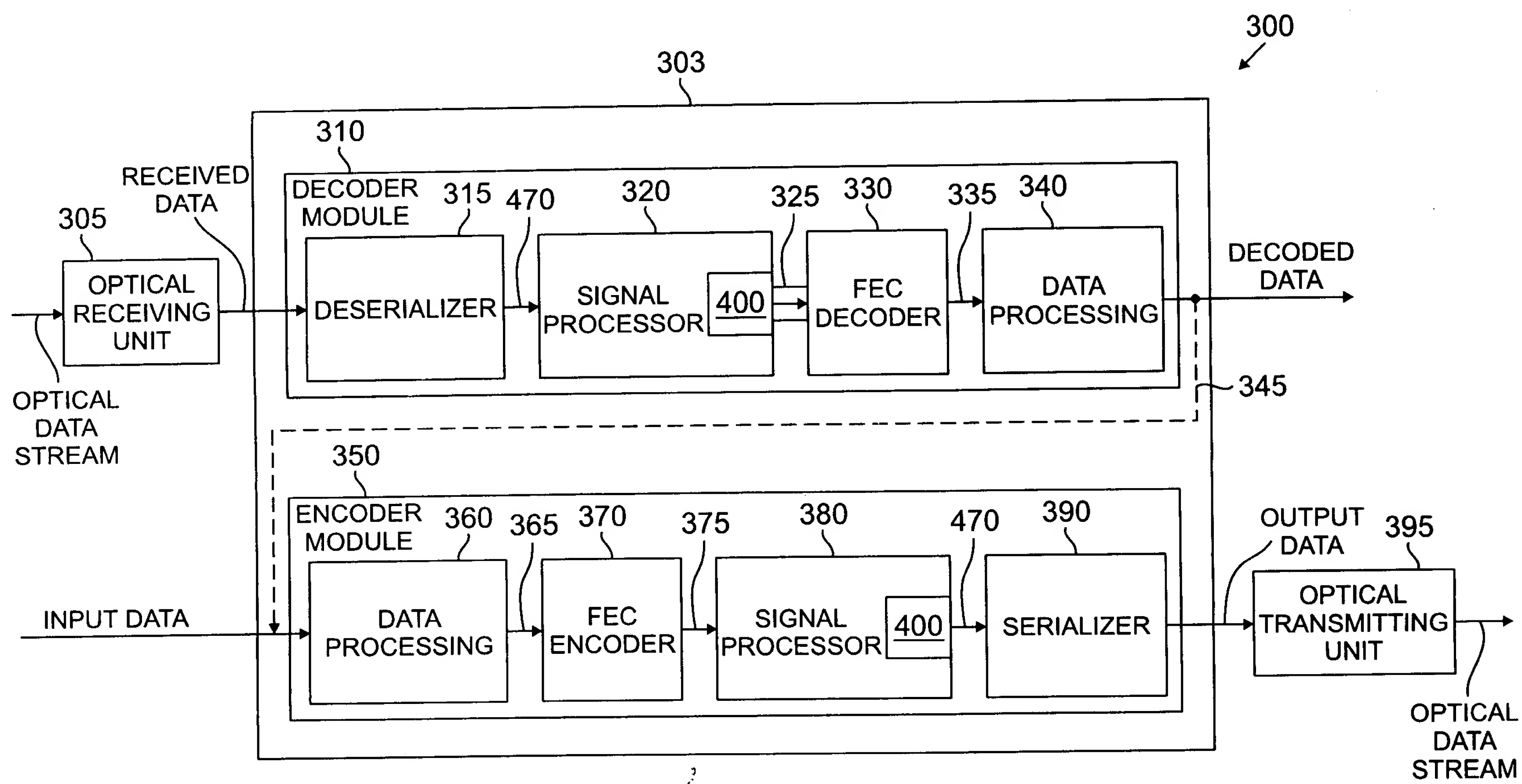

300
303
310
DECODER MODULE
315
470
320
325
330
335
340
305
RECEIVED DATA
OPTICAL RECEIVING UNIT
OPTICAL DATA STREAM
DESERIALIZER
SIGNAL PROCESSOR
400
FEC DECODER
DATA PROCESSING
DECODED DATA
345
350
ENCODER MODULE
360
365
370
375
380
470
390
INPUT DATA
DATA PROCESSING
FEC ENCODER
SIGNAL PROCESSOR
400
SERIALIZER
OUTPUT DATA
395
OPTICAL TRANSMITTING UNIT
OPTICAL DATA STREAM

FIG. 3

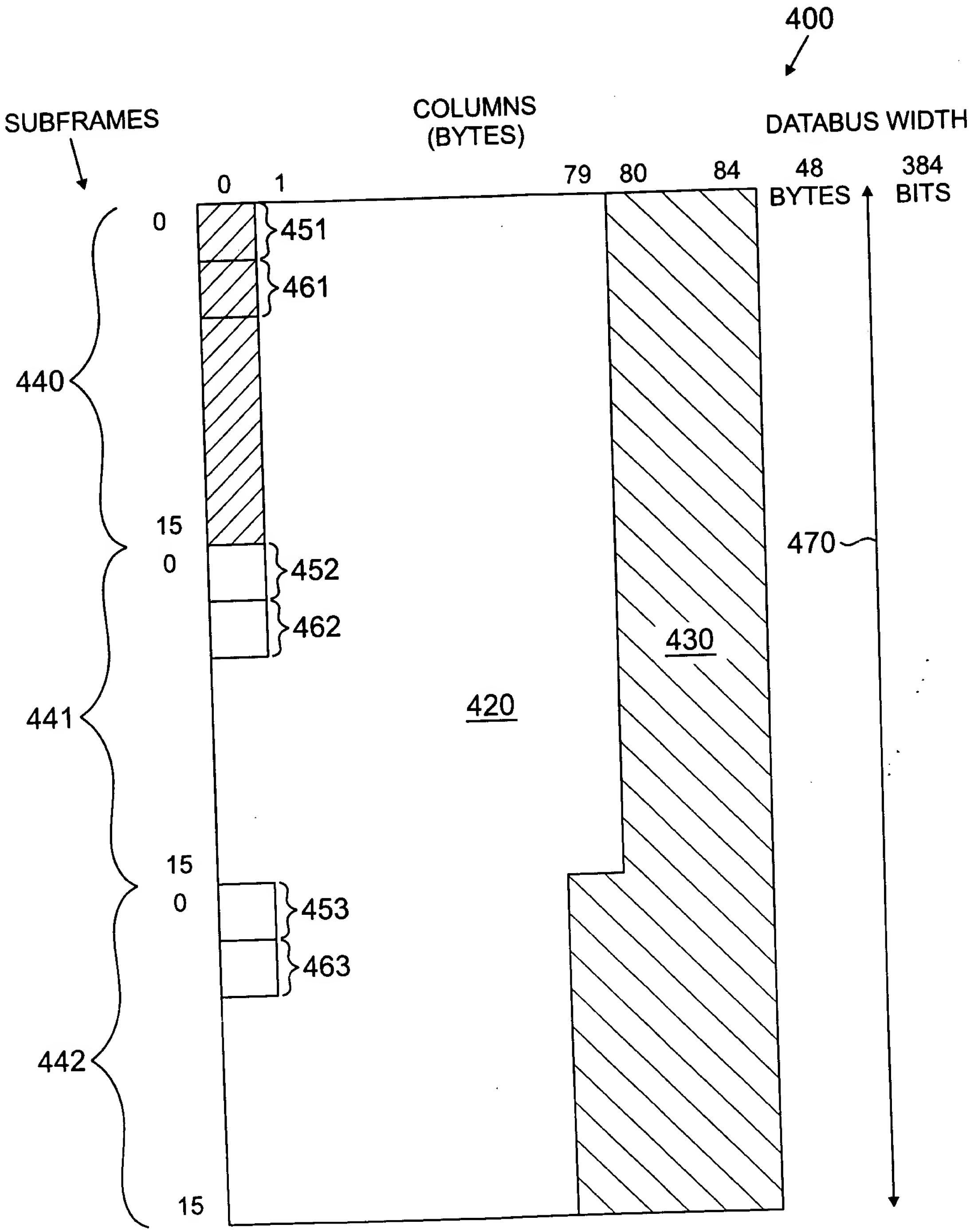

400
SUBFRAMES
COLUMNS
(BYTES)
DATABUS WIDTH
0
1
79
80
84
48
BYTES
384
BITS
0
451
461
440
15
0
452
462
430
420
441
470
15
0
453
463
442
15

FIG. 4

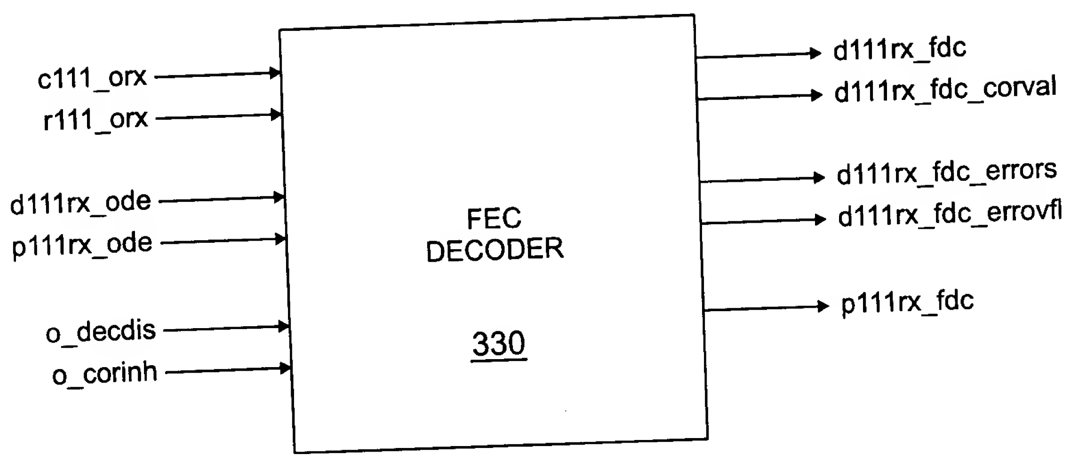

c111_orx
r111_orx
d111rx_ode
p111rx_ode
o_decdis
o_corinh
FEC
DECODER
330
d111rx_fdc
d111rx_fdc_corval
d111rx_fdc_errors
d111rx_fdc_errovfl
p111rx_fdc

FIG. 5

NAME	DIRECTION	WIDTH	DESCRIPTION
c111_orx	IN	std_ulogic	SYSTEM CLOCK, 111 MHz
r111_orx	IN	std_ulogic	SIGNAL FOR SYNCHRONOUS RESET OF DECODER
d111rx_ode	IN	(383 DOWN TO 0)	INPUT ENCODED DATA
p111rx_ode	IN	std_ulogic	START OF INPUT FEC BLOCK PULSE
o_decdis	IN	std_ulogic	DECODER FUNCTION ENABLE ('1' = DECODER IS DISABLED)
o_corinh	IN	std_ulogic	ERROR CORRECTION ENABLE ('1' = ERROR CORRECTION INHIBITED)
d111rx_fdc	BUFFER	(383 DOWN TO 0)	OUTPUT DECODED DATA
d111rx_fdc_corval	BUFFER	(383 DOWN TO 0)	OUTPUT CORRECTION VALUES: THIS SIGNAL INDICATES THE BIT POSITION IN THE DATA STREAM d111rx_fdc WHERE A BIT HAS BEEN CORRECTED (VALUES: '0' = NO CORRECTION; '1' = CORRECTION)
p111rx_fdc	BUFFER	std_logic	PULSE INDICATING THE START OF AN OUTPUT FEC BLOCK
d111rx_fdc_errors	BUFFER	(10 DOWN TO 0)	NUMBER OF CORRECTED BIT ERRORS WITHIN ONE FRAME
d111rx_fdc_errovfl	BUFFER	(4 DOWN TO 0)	NUMBER OF UNCORRECTABLE BLOCKS WITHIN ONE FRAME

FIG. 6

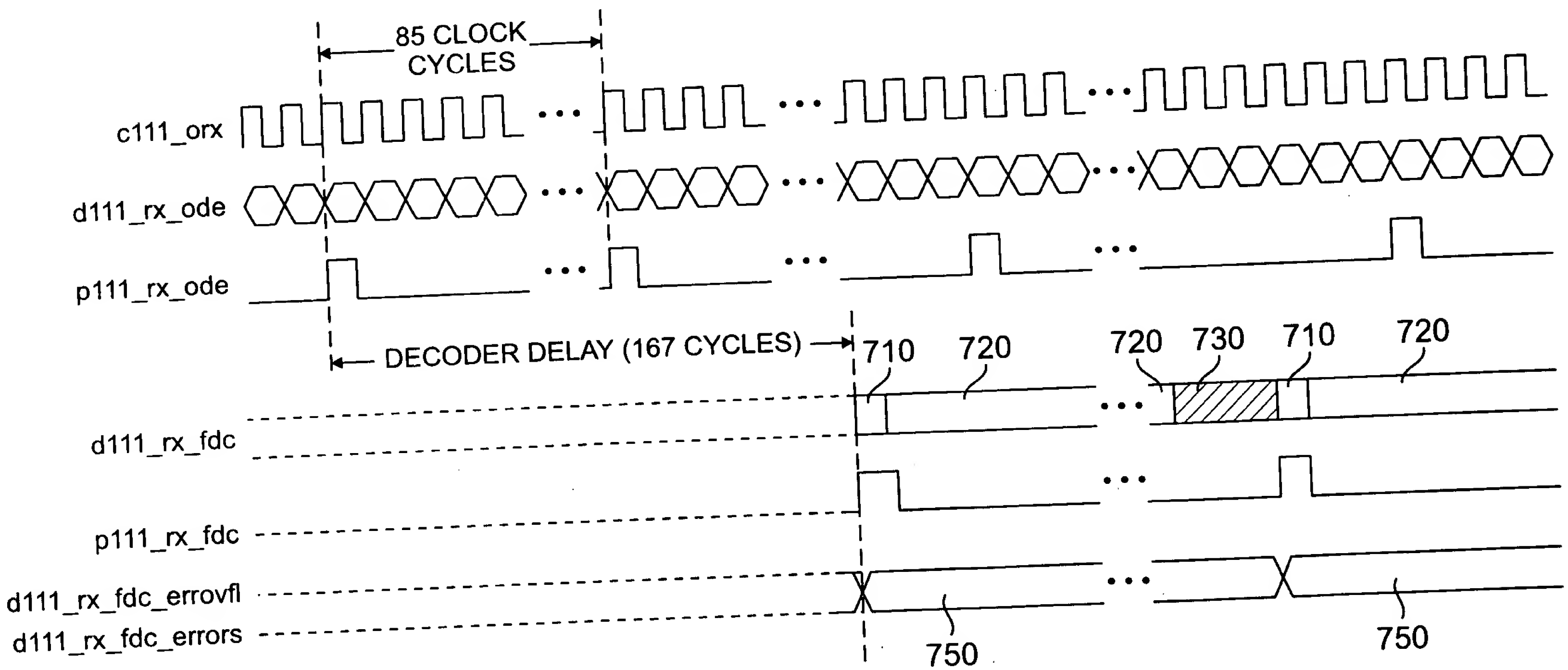

85 CLOCK CYCLES
c111_orx
d111_rx_ode
p111_rx_ode
DECODER DELAY (167 CYCLES)
710
720
720
730
710
720
d111_rx_fdc
p111_rx_fdc
d111_rx_fdc_errovfl
d111_rx_fdc_errors
750
750

FIG. 7

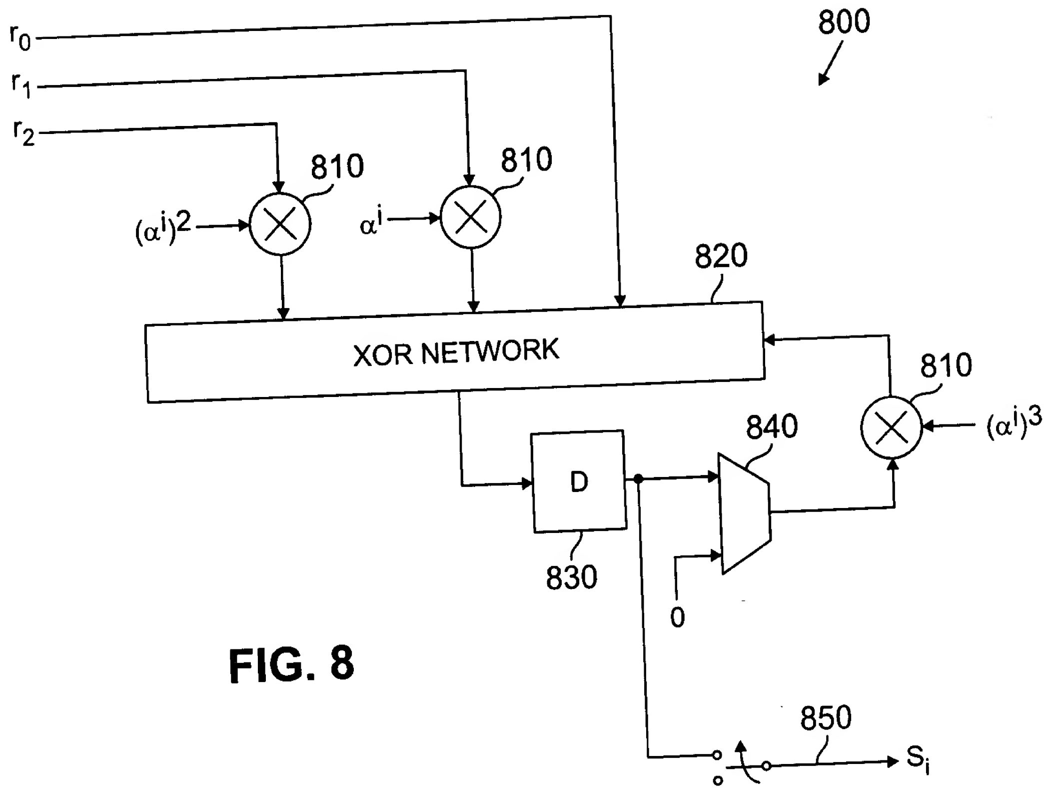

800
r_0
r_1
r_2
810
810
$(\alpha^i)^2$
α^i
820
XOR NETWORK
810
$(\alpha^i)^3$
840
D
830
0
850
S_i

FIG. 8

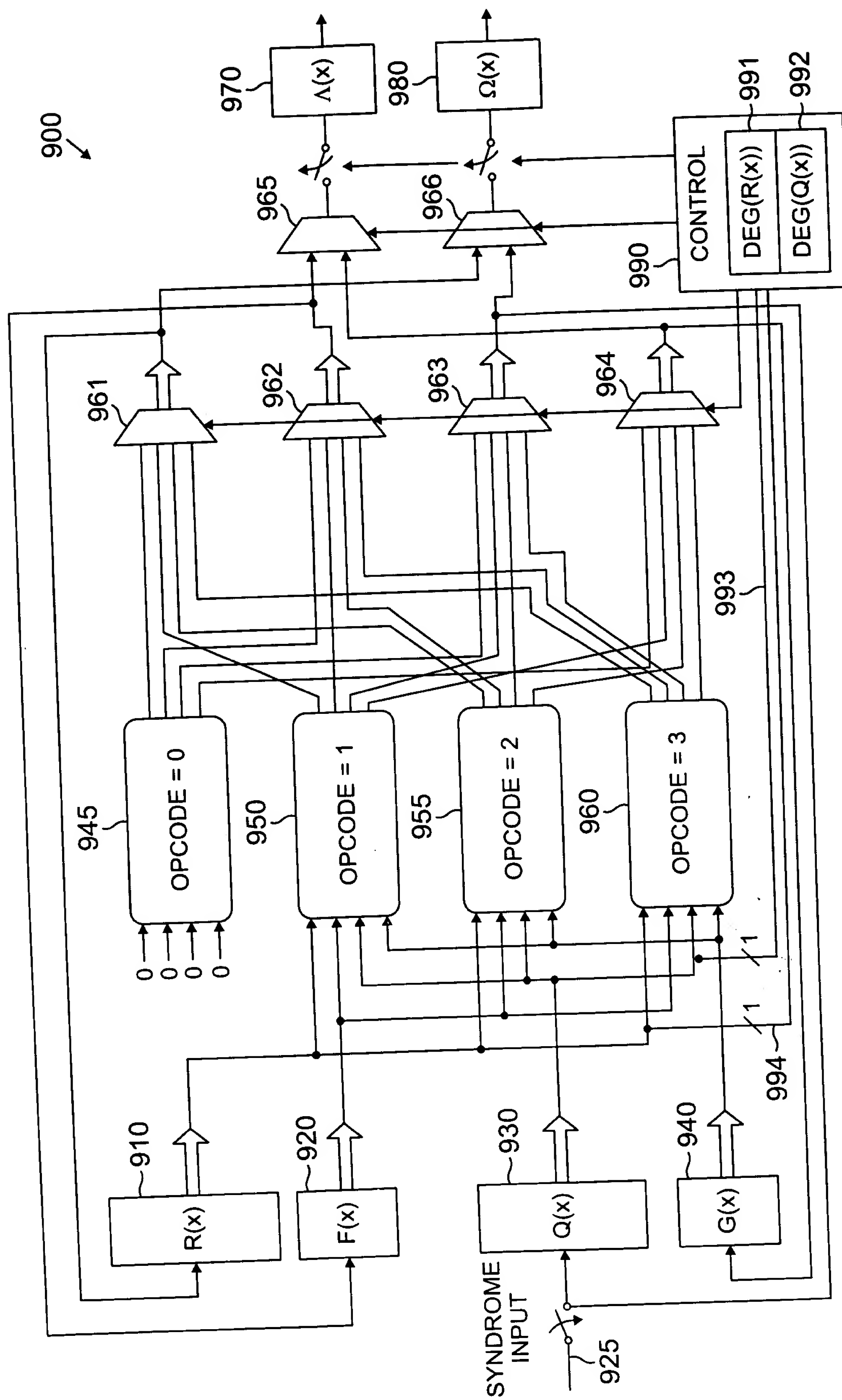

900
970
Λ(x)
980
Ω(x)
965
966
990
CONTROL
991
992
DEG(R(x))
DEG(Q(x))
961
962
963
964
945
OPCODE = 0
950
OPCODE = 1
955
OPCODE = 2
960
OPCODE = 3
993
994
1
1
0
0
0
0
910
R(x)
920
F(x)
930
Q(x)
940
G(x)
SYNDROME INPUT
925

FIG. 9

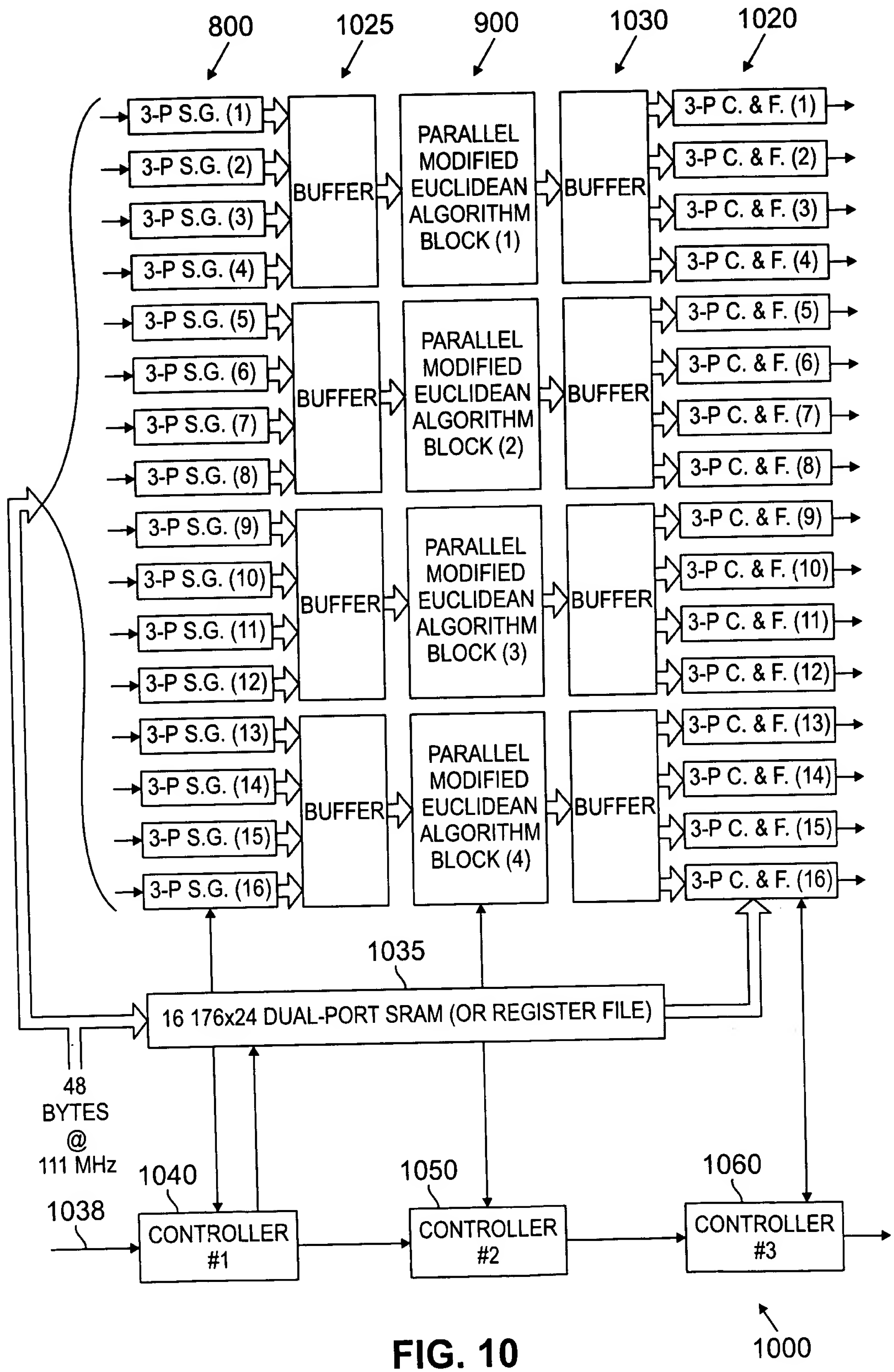

800
1025
900
1030
1020
3-P S.G. (1)
3-P S.G. (2)
3-P S.G. (3)
3-P S.G. (4)
3-P S.G. (5)
3-P S.G. (6)
3-P S.G. (7)
3-P S.G. (8)
3-P S.G. (9)
3-P S.G. (10)
3-P S.G. (11)
3-P S.G. (12)
3-P S.G. (13)
3-P S.G. (14)
3-P S.G. (15)
3-P S.G. (16)
BUFFER
PARALLEL MODIFIED EUCLIDEAN ALGORITHM BLOCK (1)
PARALLEL MODIFIED EUCLIDEAN ALGORITHM BLOCK (2)
PARALLEL MODIFIED EUCLIDEAN ALGORITHM BLOCK (3)
PARALLEL MODIFIED EUCLIDEAN ALGORITHM BLOCK (4)
3-P C. & F. (1)
3-P C. & F. (2)
3-P C. & F. (3)
3-P C. & F. (4)
3-P C. & F. (5)
3-P C. & F. (6)
3-P C. & F. (7)
3-P C. & F. (8)
3-P C. & F. (9)
3-P C. & F. (10)
3-P C. & F. (11)
3-P C. & F. (12)
3-P C. & F. (13)
3-P C. & F. (14)
3-P C. & F. (15)
3-P C. & F. (16)
1035
16 176x24 DUAL-PORT SRAM (OR REGISTER FILE)
48 BYTES @ 111 MHz
1038
1040
CONTROLLER #1
1050
CONTROLLER #2
1060
CONTROLLER #3
1000

FIG. 10

1100

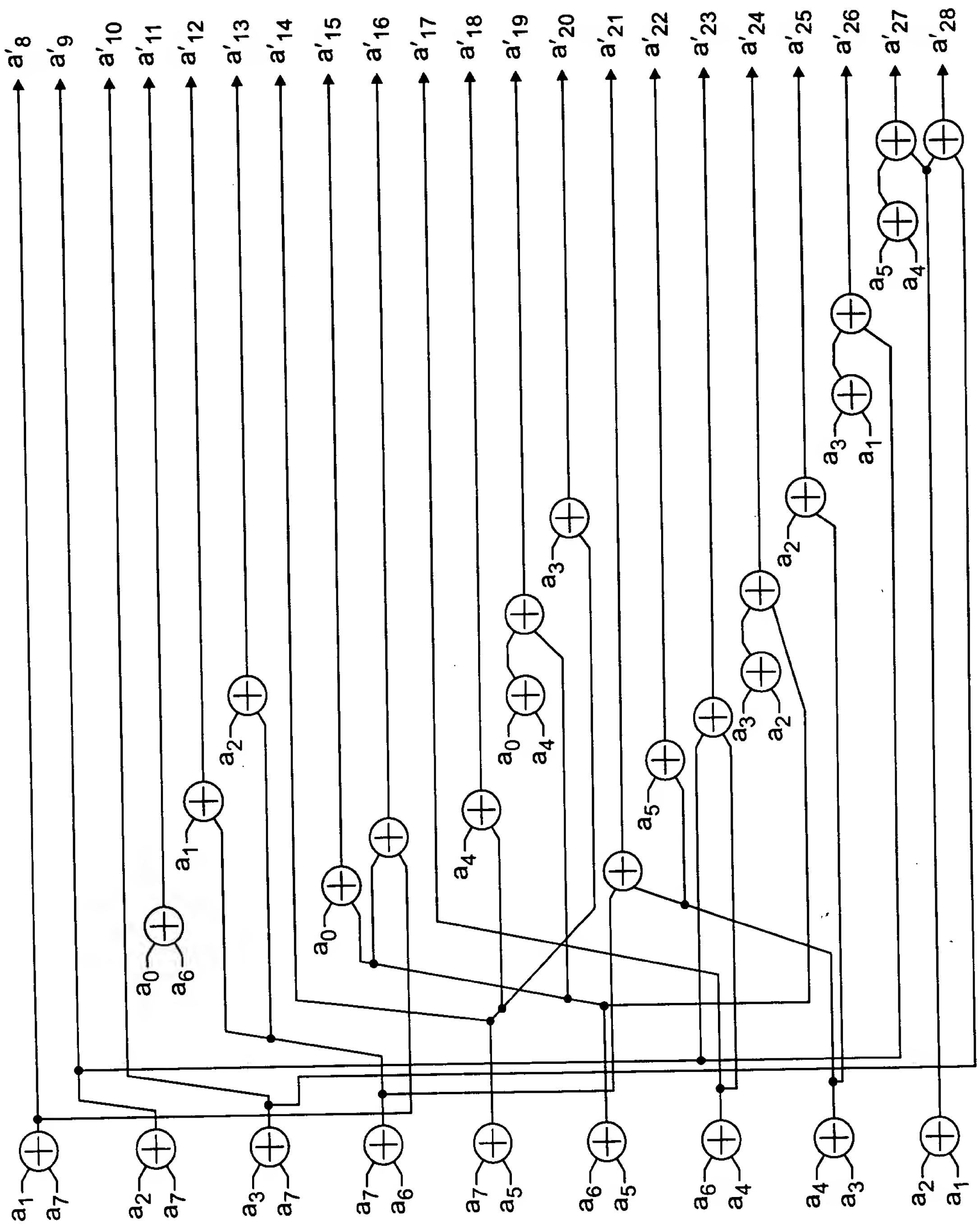

a'_8 a'_9 a'_{10} a'_{11} a'_{12} a'_{13} a'_{14} a'_{15} a'_{16} a'_{17} a'_{18} a'_{19} a'_{20} a'_{21} a'_{22} a'_{23} a'_{24} a'_{25} a'_{26} a'_{27} a'_{28}
a_1 a_7
a_2 a_7
a_3 a_7
a_7 a_6
a_7 a_5
a_6 a_5
a_6 a_4
a_4 a_3
a_2 a_1
a_0 a_6
a_1
a_2
a_0
a_4
a_0 a_4
a_3
a_5
a_3 a_2
a_2
a_3 a_1
a_5 a_4

FIG. 11

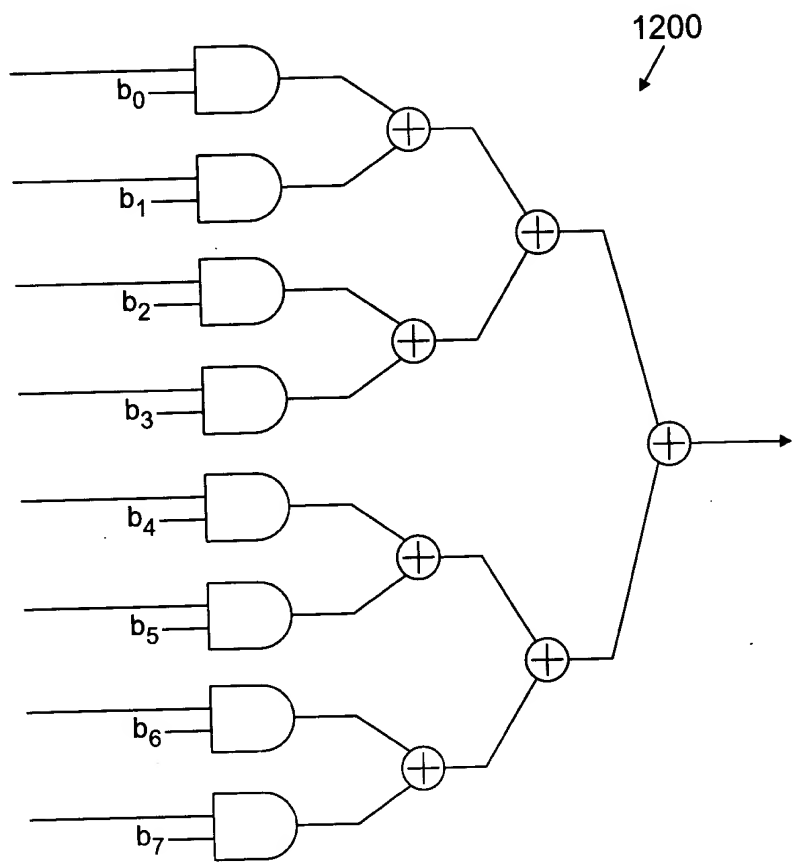


FIG. 12

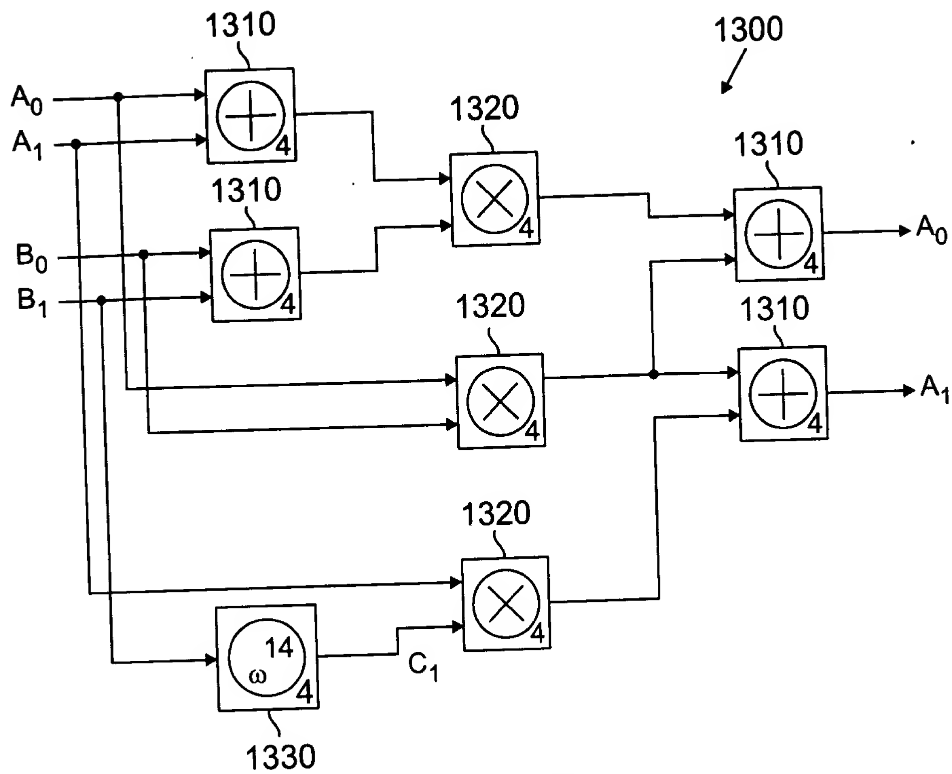


FIG. 13A

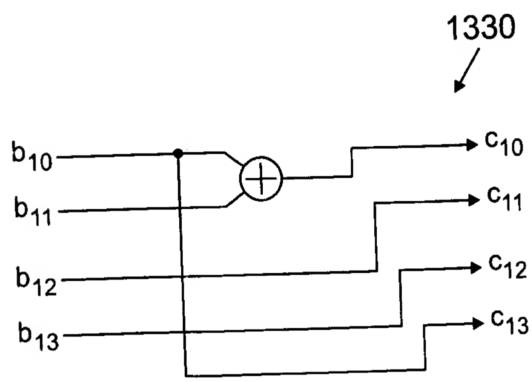


FIG. 13B

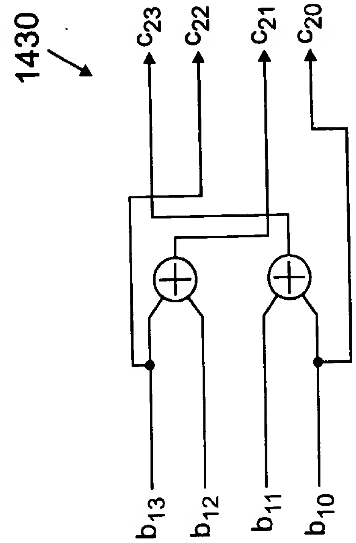


FIG. 14B

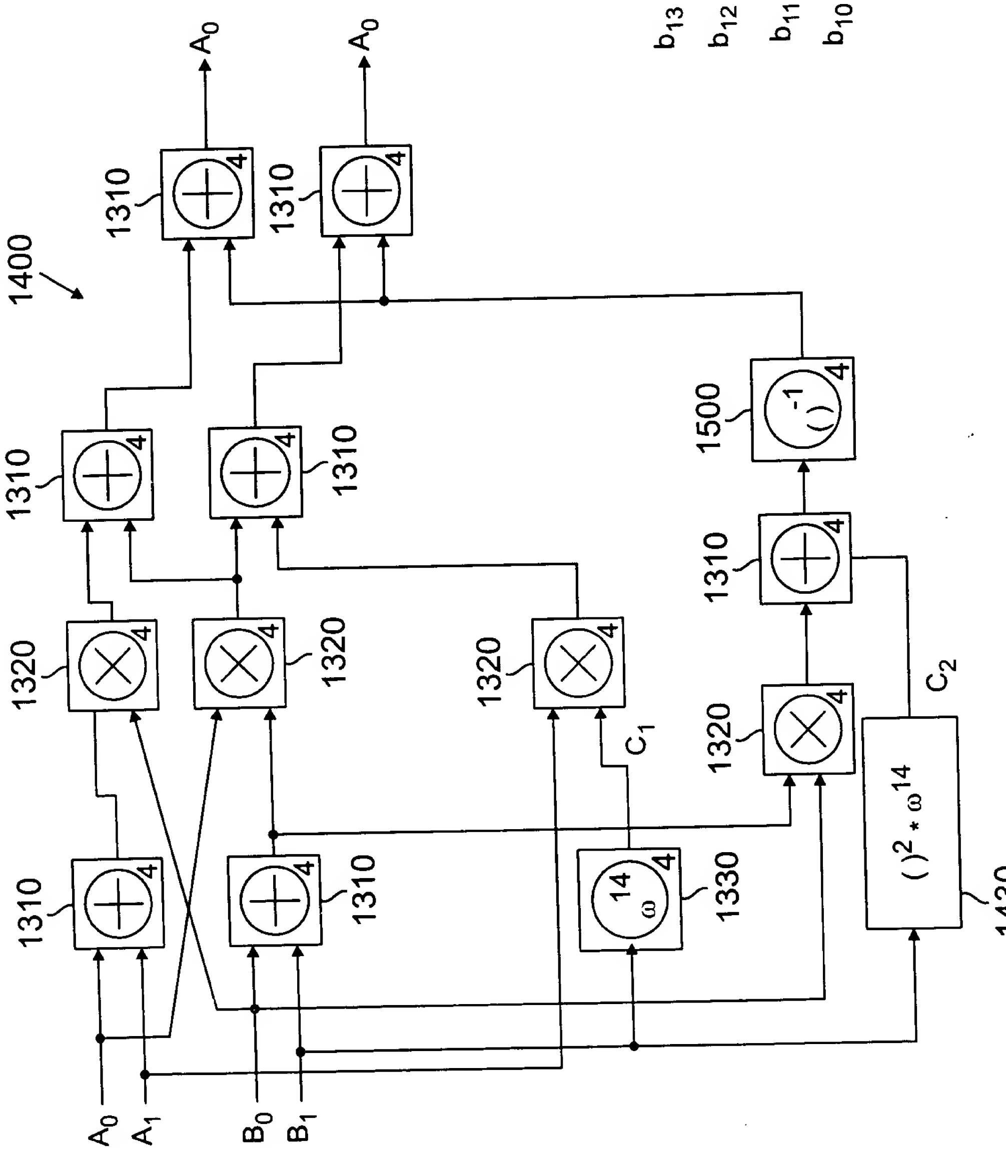


FIG. 14A

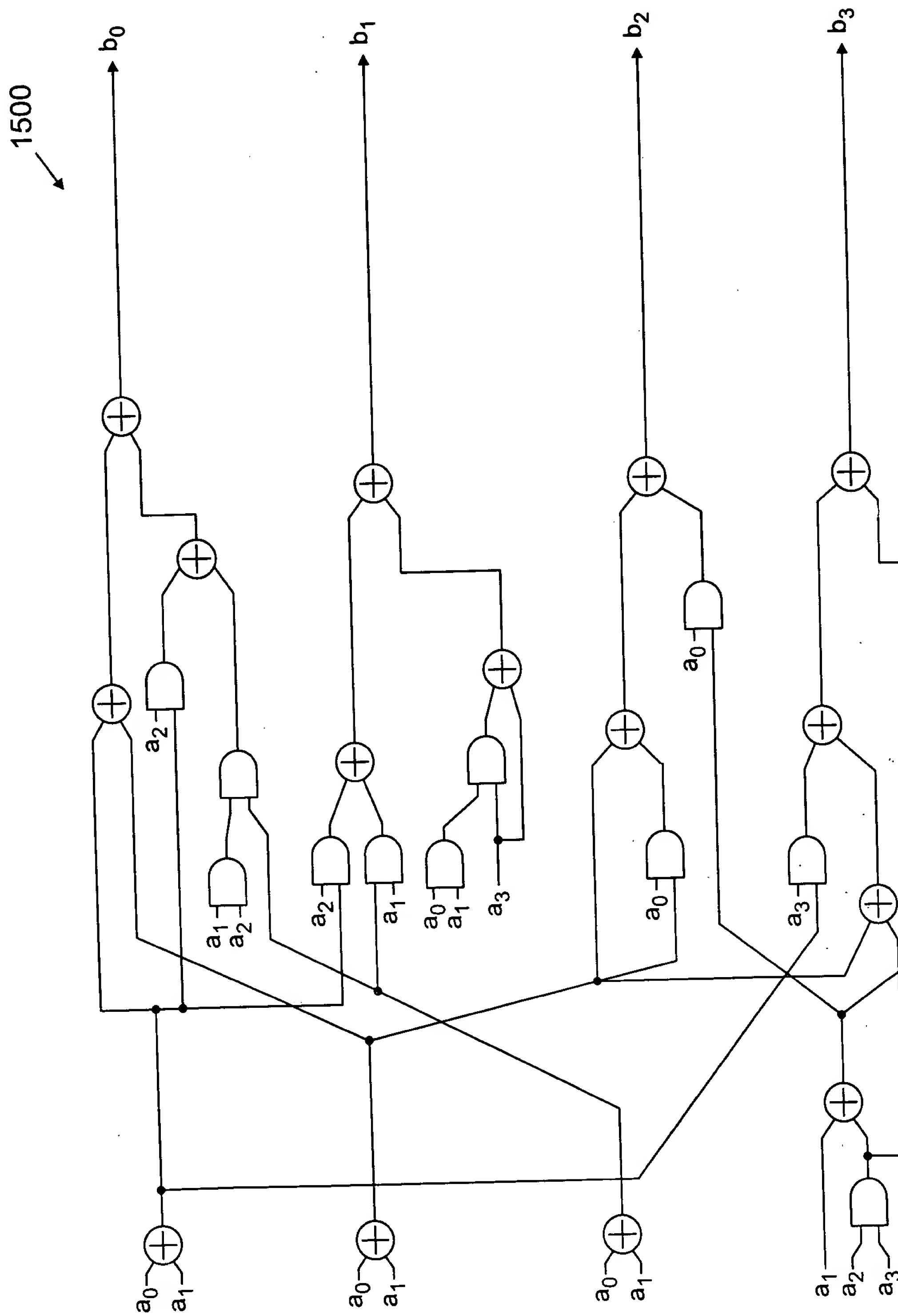


FIG. 15

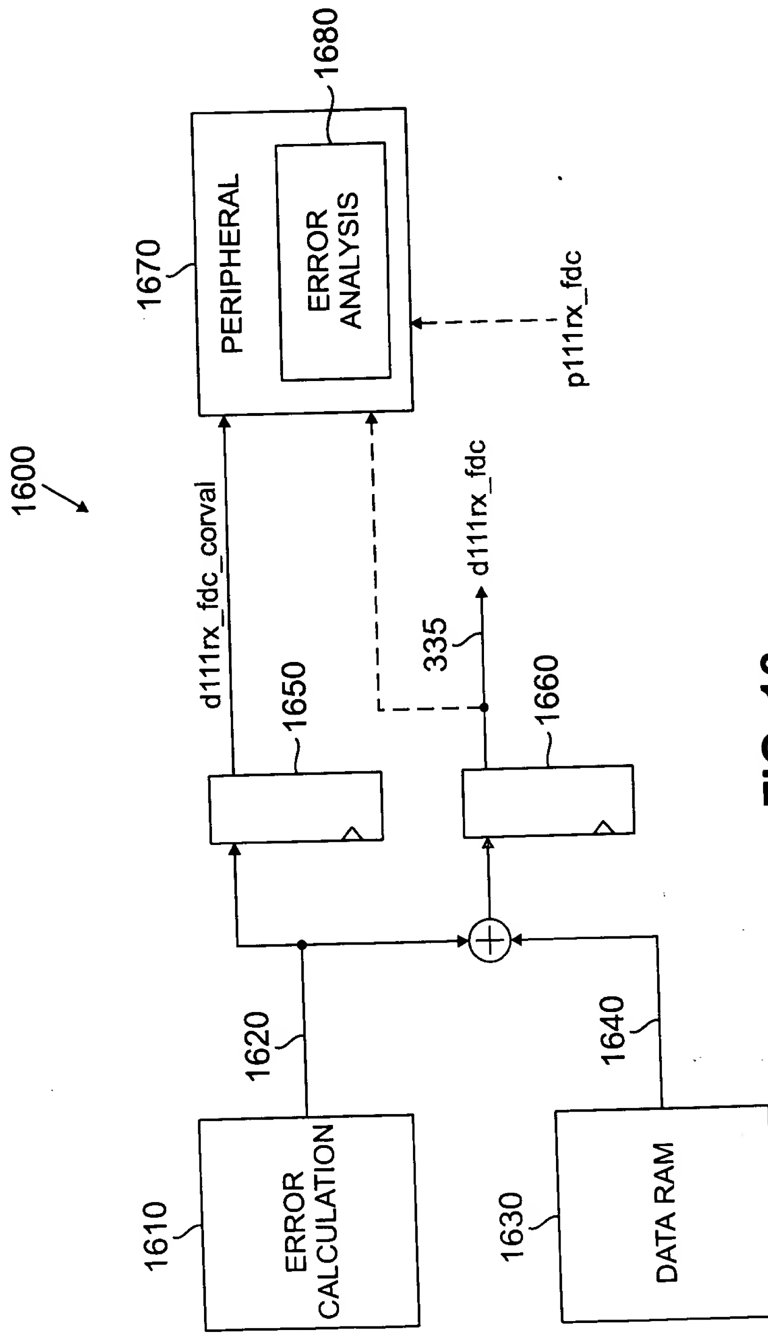

1600
1670
PERIPHERAL
1680
ERROR
ANALYSIS
p111rx_fdc
d111rx_fdc_corval
d111rx_fdc
335
1650
1660
1620
1640
1610
ERROR
CALCULATION
1630
DATA RAM

FIG. 16

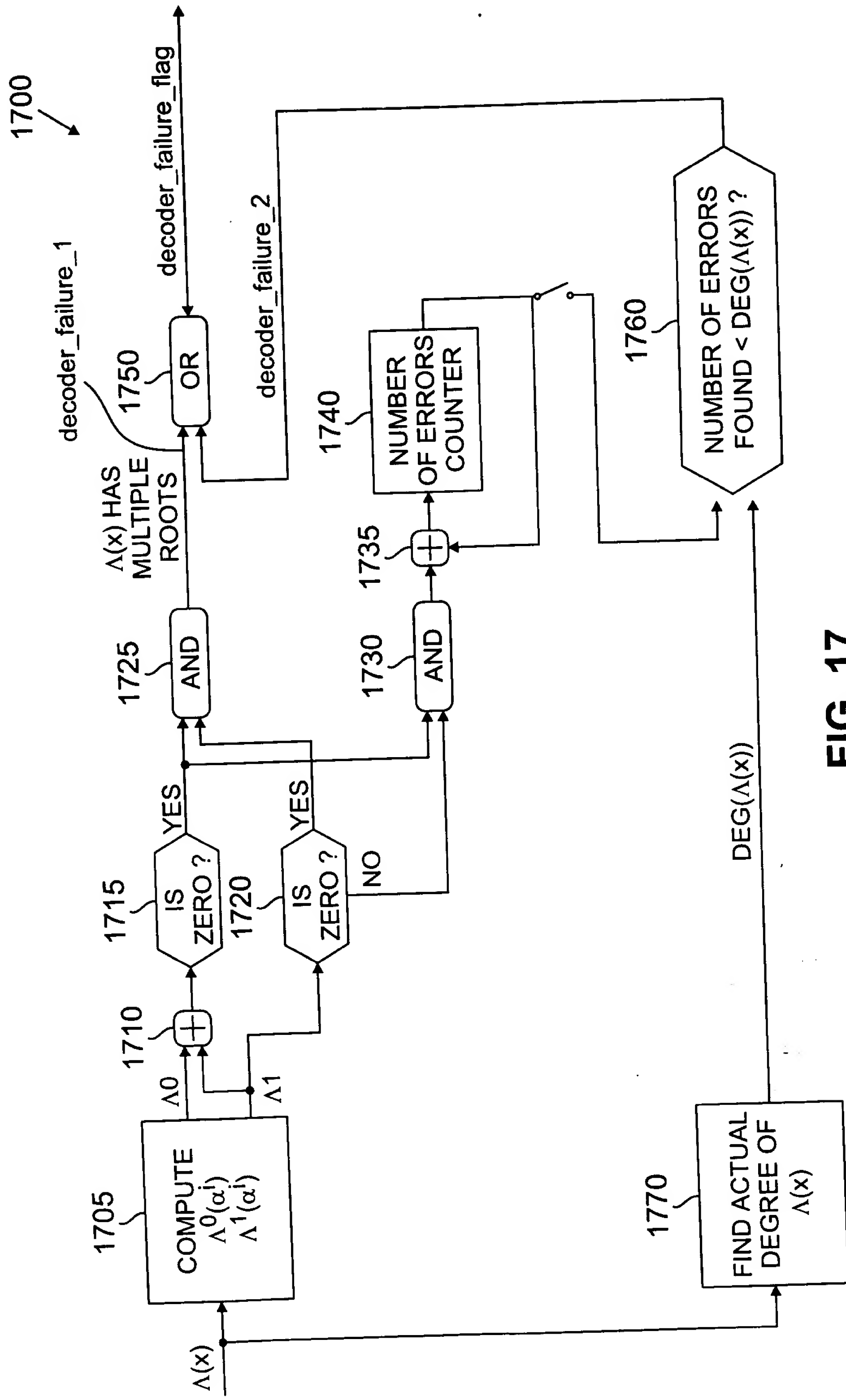

1700
decoder_failure_flag
decoder_failure_1
decoder_failure_2
1750
OR
Λ(x) HAS MULTIPLE ROOTS
1725
AND
1715
IS ZERO ?
YES
1720
IS ZERO ?
YES
NO
1710
Λ0
Λ1
1705
COMPUTE Λ0(αi) Λ1(αi)
Λ(x)
1740
NUMBER OF ERRORS COUNTER
1735
1730
AND
1760
NUMBER OF ERRORS FOUND < DEG(Λ(x)) ?
DEG(Λ(x))
1770
FIND ACTUAL DEGREE OF Λ(x)

FIG. 17

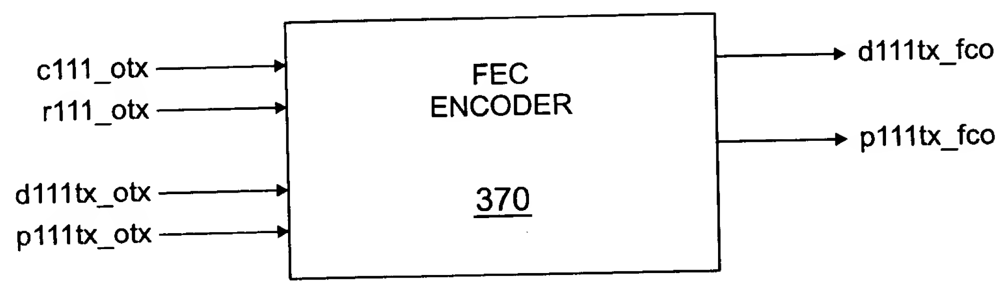


FIG. 18

NAME	DIRECTION	WIDTH	DESCRIPTION
c111_otx	IN	std_ulogic	SYSTEM CLOCK, 111 MHz
r111_otx	IN	std_ulogic	SIGNAL FOR SYNCHRONOUS RESET OF ENCODER
d111tx_otx	IN	(383 DOWN TO 0)	INPUT DATA
p111tx_otx	IN	std_ulogic	START OF INPUT FEC BLOCK PULSE
d111tx_fco	BUFFER	(383 DOWN TO 0)	OUTPUT ENCODED DATA
p111tx_fco	BUFFER	std_ulogic	PULSE INDICATING THE END OF AN FEC BLOCK

FIG. 19

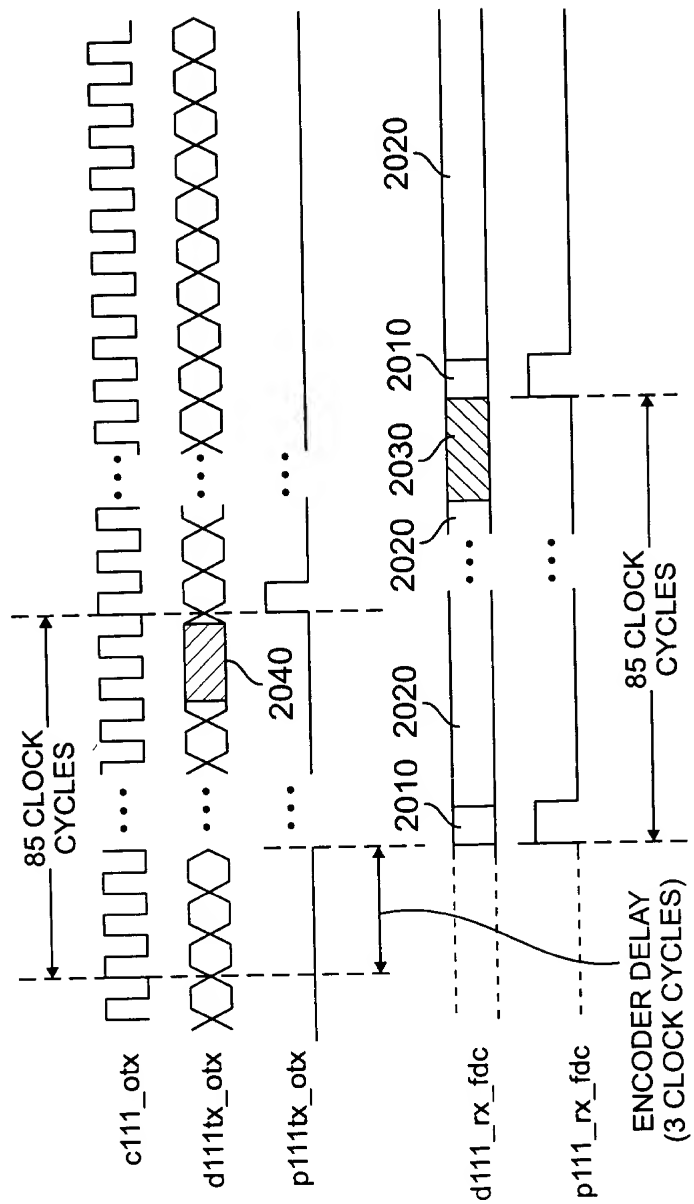

c111_otx
d111tx_otx
p111tx_otx
d111_rx_fdc
p111_rx_fdc
85 CLOCK CYCLES
2040
2010
2020
2030
2010
2020
85 CLOCK CYCLES
ENCODER DELAY (3 CLOCK CYCLES)

FIG. 20

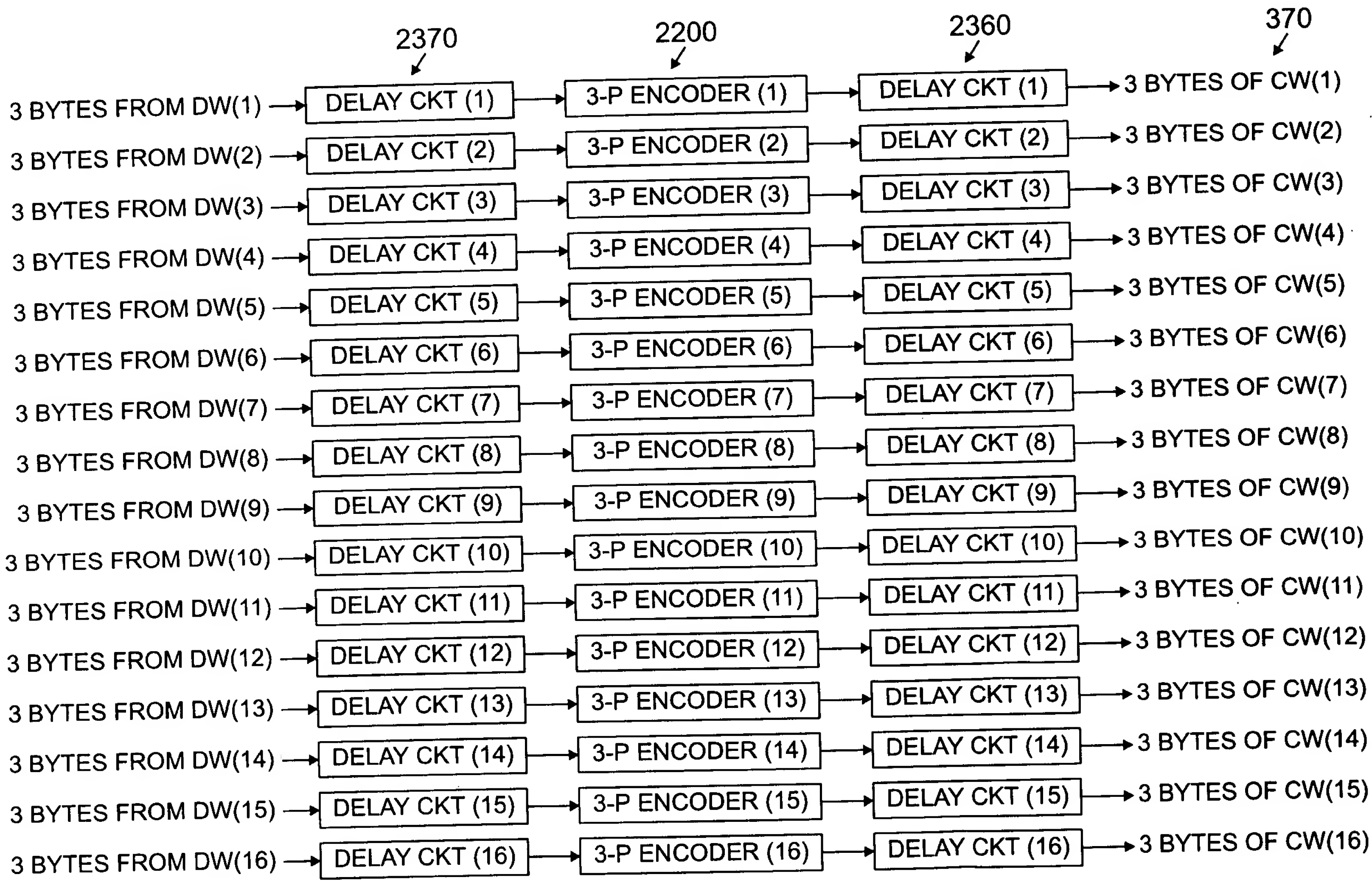
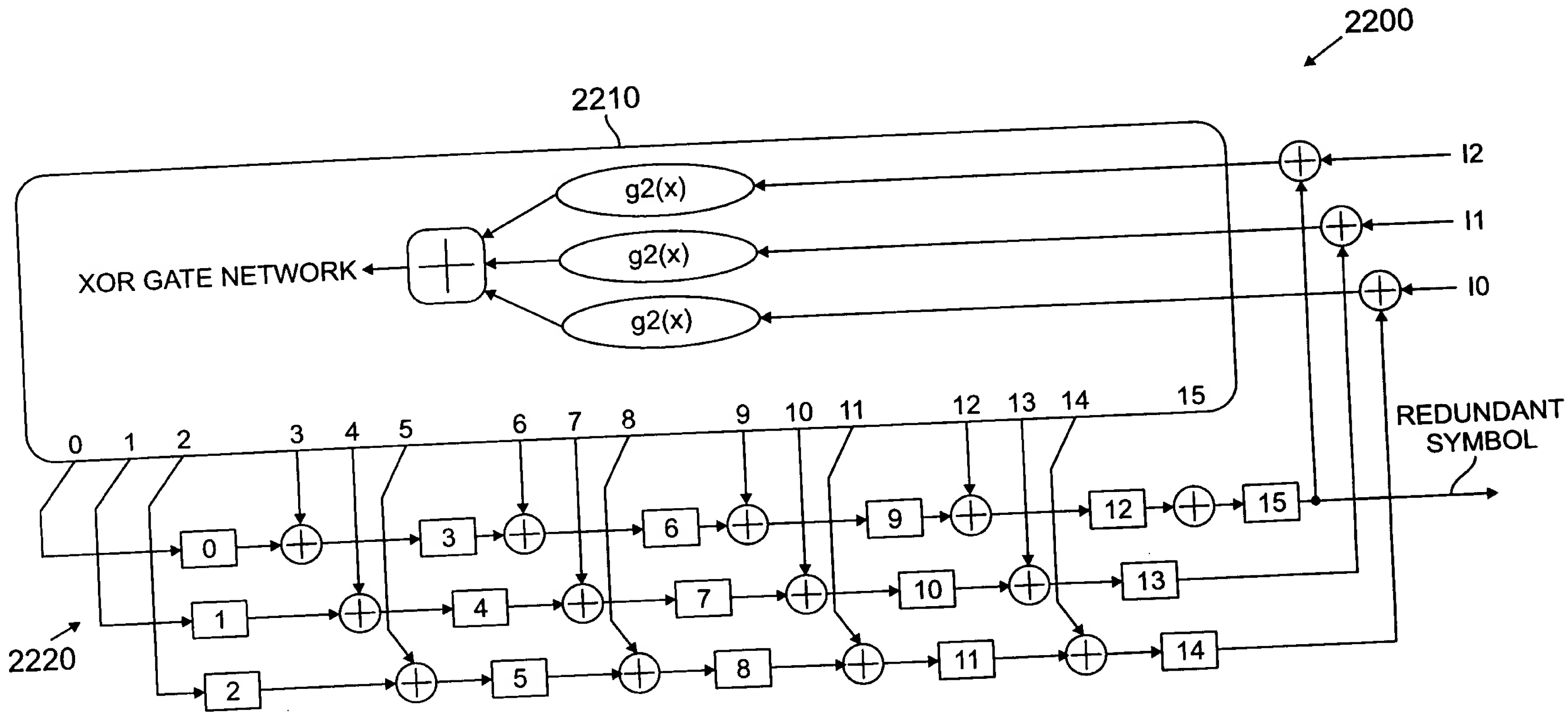

2370
2200
2360
370
3 BYTES FROM DW(1)
DELAY CKT (1)
3-P ENCODER (1)
DELAY CKT (1)
3 BYTES OF CW(1)
3 BYTES FROM DW(2)
DELAY CKT (2)
3-P ENCODER (2)
DELAY CKT (2)
3 BYTES OF CW(2)
3 BYTES FROM DW(3)
DELAY CKT (3)
3-P ENCODER (3)
DELAY CKT (3)
3 BYTES OF CW(3)
3 BYTES FROM DW(4)
DELAY CKT (4)
3-P ENCODER (4)
DELAY CKT (4)
3 BYTES OF CW(4)
3 BYTES FROM DW(5)
DELAY CKT (5)
3-P ENCODER (5)
DELAY CKT (5)
3 BYTES OF CW(5)
3 BYTES FROM DW(6)
DELAY CKT (6)
3-P ENCODER (6)
DELAY CKT (6)
3 BYTES OF CW(6)
3 BYTES FROM DW(7)
DELAY CKT (7)
3-P ENCODER (7)
DELAY CKT (7)
3 BYTES OF CW(7)
3 BYTES FROM DW(8)
DELAY CKT (8)
3-P ENCODER (8)
DELAY CKT (8)
3 BYTES OF CW(8)
3 BYTES FROM DW(9)
DELAY CKT (9)
3-P ENCODER (9)
DELAY CKT (9)
3 BYTES OF CW(9)
3 BYTES FROM DW(10)
DELAY CKT (10)
3-P ENCODER (10)
DELAY CKT (10)
3 BYTES OF CW(10)
3 BYTES FROM DW(11)
DELAY CKT (11)
3-P ENCODER (11)
DELAY CKT (11)
3 BYTES OF CW(11)
3 BYTES FROM DW(12)
DELAY CKT (12)
3-P ENCODER (12)
DELAY CKT (12)
3 BYTES OF CW(12)
3 BYTES FROM DW(13)
DELAY CKT (13)
3-P ENCODER (13)
DELAY CKT (13)
3 BYTES OF CW(13)
3 BYTES FROM DW(14)
DELAY CKT (14)
3-P ENCODER (14)
DELAY CKT (14)
3 BYTES OF CW(14)
3 BYTES FROM DW(15)
DELAY CKT (15)
3-P ENCODER (15)
DELAY CKT (15)
3 BYTES OF CW(15)
3 BYTES FROM DW(16)
DELAY CKT (16)
3-P ENCODER (16)
DELAY CKT (16)
3 BYTES OF CW(16)

FIG. 21



2200
2210
XOR GATE NETWORK
g2(x)
g2(x)
g2(x)
I2
I1
I0
REDUNDANT SYMBOL
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
2220

FIG. 22

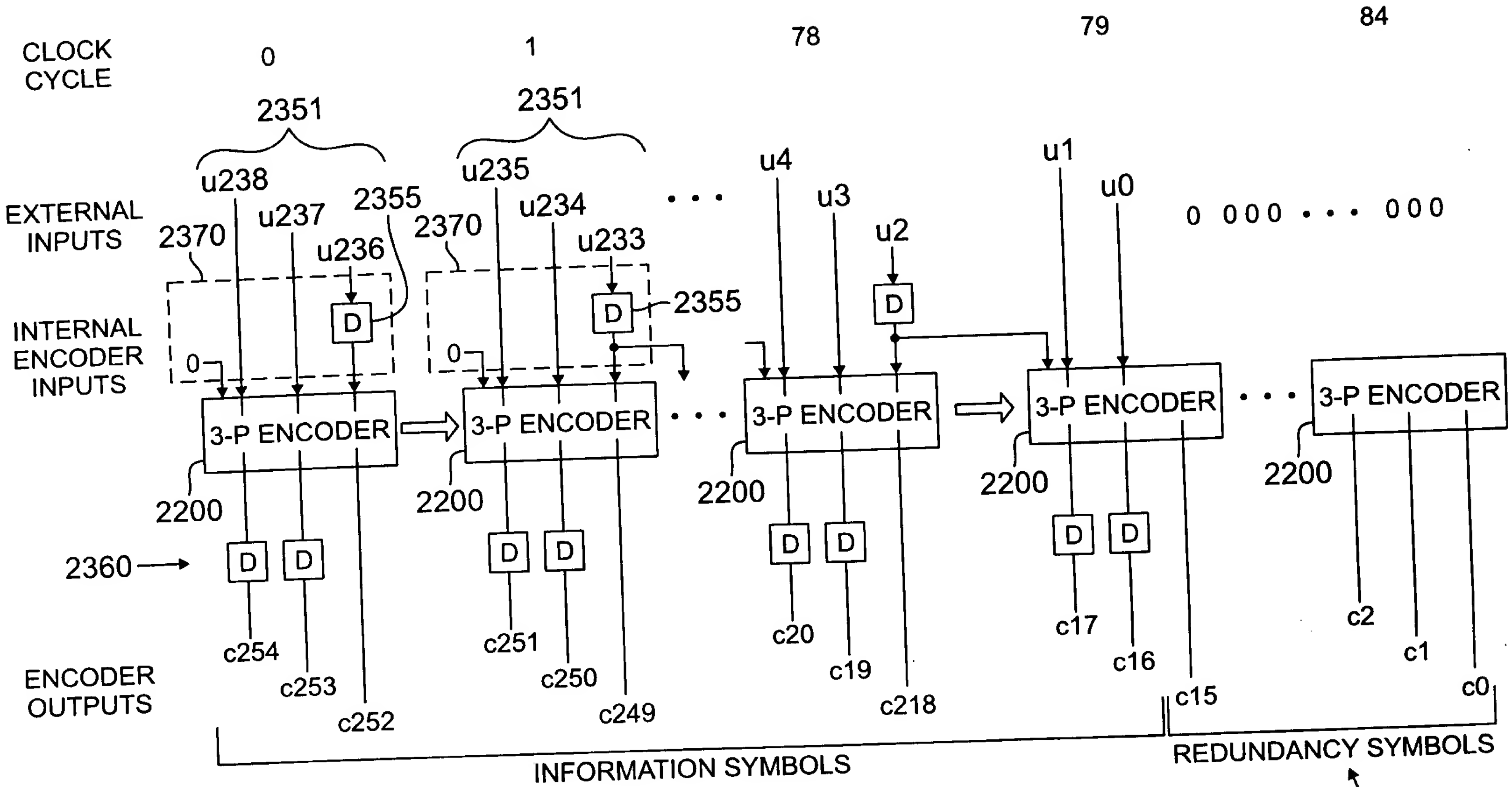

CLOCK CYCLE
0
1
78
79
84
EXTERNAL INPUTS
INTERNAL ENCODER INPUTS
2351
2351
u238
u237
u236
2355
2370
u235
u234
u233
2355
2370
u4
u3
u2
u1
u0
0 000 • • • 000
0
0
D
3-P ENCODER
2200
2360
ENCODER OUTPUTS
c254
c253
c252
c251
c250
c249
c20
c19
c218
c17
c16
c15
c2
c1
c0
INFORMATION SYMBOLS
REDUNDANCY SYMBOLS
2300

FIG. 23